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in the following listed application(s) or patent(s) for which the issue fee has been paid.

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Respectfully Submitted,



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(12) **United States Patent**
Nakamura

(10) **Patent No.:** US 7,554,117 B2
(45) **Date of Patent:** Jun. 30, 2009

(54) **SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF**

(75) Inventor: Osamu Nakamura, Atsugi (JP)

(73) Assignee: Semiconductor Energy Laboratory Co., Ltd. (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 841 days.

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(58) Field of Classification Search 257/59, 257/72, 347, E27.112, E29.117

See application file for complete search history.

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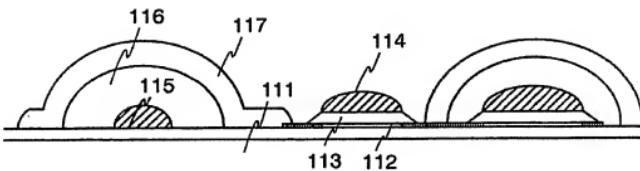
ABSTRACT

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An island-like interlayer insulating film is formed selectively in a region where a source interconnection and a gate interconnection intersect. For example, by use of ink jet method, a solution containing an insulating material is dropped on a region where the gate interconnection and the source interconnection intersect or a region where a holding capacitor is formed, that enable to reduce a photolithography process and to reduce the number of masks that are used in a TFT.

18 Claims, 7 Drawing Sheets



(intersection of interconnections)

(TFT)

(holding capacitor)